SEMICONDUCTOR MEMORY WITH EMBEDDED DRAM

ABSTRACT

A semiconductor memory comprises a plurality of memory cells, for example Flash memory cells, arranged in a plurality of lines, and a plurality of memory cell access signal lines, each one associated with at least one respective line of memory cells, for accessing the memory cells of the at least one respective line of memory cells; each signal line has a capacitance intrinsically associated therewith. A plurality of volatile memory cells is provided, each having a capacitive storage element. Each volatile memory cell is associated with a respective signal line, and the respective capacitive storage element formed by the capacitance intrinsically associated with the respective signal lines. In particular, the parasitic capacitances associated with bit lines of a matrix of memory cells can be exploited as capacitive storage elements.